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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/731,060	12/07/2000	Edward Colles Nevill	550-192	1332

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EXAMINER	
ZHEN, LI B	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,060	NEVILL ET AL.	
	Examiner	Art Unit	
	Li B. Zhen	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/01;11/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 16 are pending in the application.

Information Disclosure Statement

2. The reference, "A Pipeline Push-Down Stack Computer," is not legible except for the title and section headings. Examiner was only able to consider the legible sections, mainly the title and the section headings. A clean copy of the reference is required for full consideration of the text of the reference.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 2, 7, 11 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,937,193 to Evoy in view of U.S. Patent No. 5,875,336 to Dickol et al. [hereinafter referred to as Dickol].**

6. As to claim 1, Evoy teaches the invention substantially as claimed including an apparatus [computer system 10, Fig. 1; col. 3, lines 29 – 42] for processing data operable to execute operations specified in a stream of program instructions [converting platform-independent instructions to be executed by a processor into corresponding native instructions for the processor; col. 4, lines 9 – 20 and col. 3, lines 42 – 60], the apparatus comprising:

(i) a hardware based instruction execution unit operable to execute program instructions [a translation circuit 50 coupled to system data bus 24 is utilized to receive 8-bit Java bytecodes and output corresponding 32-bit native instructions directly to processor 40 for execution; col. 4, lines 52 – 62]; and

(ii) a software based instruction execution unit [software interpreter; col. 5, lines 57 – 67] operable to execute program instructions [interpret the unmapped bytecode via a software interpreter; col. 5, lines 57 – 67, col. 6, lines 1 – 8, col. 7, lines 8 – 16]; wherein

(iii) program instructions to be executed are sent to the hardware based execution unit [a platform-independent instruction (here a Java bytecode) is fetched from the memory; col. 10, lines 45 – 57] for execution [Translate Code routine 200, for translation state machine 153; col. 32 – 45]; and

(iv) program instructions received by the hardware based execution unit for which execution is not supported by the hardware based execution unit are forwarded to the software based execution unit for execution [If no corresponding native instruction exists, table 51 outputs an exception signal, which notifies processor 40 that software

interpretation of the bytecode may be required; col. 7, lines 8 – 17; col. 5, lines 57 – 67; col. 6, lines 1 – 8; col. 9, lines 54 – 65; col. 11, lines 23 – 37] with control being returned to the hardware based execution unit for a next program instruction to be executed [selecting next bytecode; col. 7, lines 8 – 16; col. 11, lines 6 – 15].

As to scheduling support logic, examiner notes that the limitation "scheduling support logic" is very broad. Scheduling functions could refer to identifying the next instructions to be executed or dispatching the next instruction to be executed. Evoy schedules instructions to be executed by the processor and dispatching the next instruction to be executed [After execution of a native instruction when in the platform-independent mode, processor 40 increments its address counter to the next instruction, which has the effect of selecting the next bytecode provided to byte select multiplexer 56; col. 7, lines 17 – 28].

7. In addition, Dickol teaches translating non-native instructions to instructions native to a processor within a computer system [col. 2, lines 28 – 33 and col. 3, lines 42 – 62] and hardware based execution unit includes scheduling support logic operable to generate a scheduling signal for triggering a scheduling operation to be performed between program instructions irrespective of whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit [branch instruction that will be passed to CPU 11 is generated by combining the opcode from an entry in Semantics Table 23 with the branch offset generated by Generate Branch Module 25; col. 6, lines 9 – 18].

8. It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply the teaching of hardware based execution unit includes scheduling support logic as taught by Dickol to the invention of Evoy because provides a hardware element that translates non-native instructions to native instructions as soon as the processor within the computer attempts to perform an instruction fetch from a system memory [col. 2, lines 9 – 18 of Dickol].

9. As to claim 16, this is a method claim that corresponds to apparatus claim 1; note the rejection to claim 1 above, which also meet this method claim.

10. As to claim 2, Evoy as modified teaches the scheduling support logic includes a counter with a value [address counter; col. 7, lines 17 – 27 of Evoy] that is changed in response to a program instruction sent to the hardware based execution unit [After execution of a native instruction when in the platform-independent mode, processor 40 increments its address counter to the next instruction; col. 7, lines 17 – 27 of Evoy].

11. As to claim 7, Evoy as modified teaches a debug operation is triggered by the scheduling signal [col. 9, lines 46 – 52 of Evoy].

12. As to claim 11, Evoy as modified teaches a processor core operable to execute operations as specified by instructions of a first instruction set [col. 4, lines 38 – 44 and col. 7, lines 50 – 61 of Evoy].

13. As to claim 12, Evoy as modified teaches the hardware based instruction execution unit includes an instruction translator operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of the first instruction set [if a corresponding native instruction to the selected bytecode exists, table 51 outputs it over data lines 54a and directly to processor 40; col. 7, lines 8 – 16 of Evoy].

14. As to claim 13, Evoy as modified teaches (i) at least one instruction of the second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of the first instruction set in order to be performed by the processor core [branch instructions; col. 5, line 65 – col. 6, line 18 of Dickol]; and

(ii) the instruction translator is operable to generate a sequence of translator output signals to control the processor core to perform the multi-step operation [col. 6, line 65 – col. 7, line 10 of Dickol].

15. As to claim 14, Evoy as modified teaches the software based execution unit is a software based interpreter [software interpreter; col. 5, lines 57 – 67 of Evoy].

16. As to claim 15, Evoy as modified teaches the program instructions are Java Virtual Machine instructions [col. 4, lines 52 – 62 of Evoy].

17. **Claims 3 – 6 and 8 – 10 are rejected over Evoy and Dickol further in view of applicant's admitted prior art [p. 2, hereinafter APA].**

18. As to claim 3 – 6, Evoy as modified does not specifically teach a counter that triggers generation of scheduling signal.

However, APA states that it is known to control processing operations using a counter base approach whereby program instructions being executed are counted and a scheduling operation initiated each time a predetermined program instruction count level is reached [page 2, lines 12-15].

19. It would have been obvious to a person of ordinarily skilled in the art at the time of the invention to apply the teaching of a counter that triggers generation of scheduling signal as taught by APA to the invention of Evoy as modified because this ensures that scheduling operations are stated at safe points between the execution of program instructions.

20. As to claim 8 – 10, Evoy as modified teaches timer based scheduling wherein a scheduling signal is combined with a timer signal to trigger scheduling [page 2, lines 15-17 of APA].

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2194

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